ABSTRACT OF THE DISCLOSURE

A video and graphics system includes a video decoding system for processing compressed video data. The compressed video data includes MPEG-2 video data containing SDTV video data or HDTV video data. The video decoding system includes a video decoder for processing the compressed video data to generate displayable video, and a memory controller for transferring the compressed video data to and from an external memory. The video decoder requests to the memory controller to transfer the compressed video data using one of predetermined addressing patterns. The predetermined addressing patterns allow for more efficient transferring of the compressed video data to and from the external memory when compared to sequentially transferring a fixed number of data bytes starting at a fixed address. The use of the predetermined addressing patterns results in reading the compressed video data from the external memory in a predetermined order in a less number of clock cycles. The use of the predetermined addressing patterns also results in transferring the compressed video data over the data bus between the memory controller and the video decoder in a less number of clock cycles.